What is claimed is:

1. A method of manufacturing a thin film transistor, comprising:

a) forming an amorphous silicon layer and a blocking layer on an insulating substrate;

b) forming a photoresist layer having first and second photoresist patterns on the blocking layer, the first and second photoresist patterns spaced apart from each other;

c) etching the blocking layer using the first photoresist pattern as a mask to form first and second blocking patterns;

d) reflowing the photoresist layer, so that the first and second photoresist patterns abut on each other to entirely cover the first and second blocking patterns;

e) forming a metal layer over an entire first surface of the insulating substrate;

f) removing the photoresist layer to expose the blocking layer and an offset region between the blocking layer and the metal layer;

g) crystallizing the amorphous silicon layer to form a poly silicon layer metal induced lateral crystallization front;

h) etching the poly silicon layer using the first and second blocking patterns as a mask to form first and second semiconductor layers and to remove the metal induced lateral crystallization front; and

i) removing the first and second blocking patterns.

2. The method of claim 1, wherein the metal layer is made of Ni or Pd and has a thickness of 1 Å to 5000 Å.

3. The method of claim 1, further comprising, after the step (i), surface-treating the first and second semiconductor layers.

4. The method of claim 3, wherein the surface treatment is performed using a dry-etching technique or an HF etching solution of 0.1 % to 20 %.

5. The method of claim 1, wherein the blocking layer is patterned using a dry-etching technique or an HF etching solution of 0.1 % to 20 %.

6. The method of claim 1, further comprising, before the step (a), forming a buffer layer on the insulating substrate.

7. The method of claim 1, further comprising, after the step (i):

j) forming a gate insulating layer over said entire first surface of the insulating substrate;

k) forming a gate electrode on the gate insulating layer over the first and second semiconductor layers;

l) forming first source and drain regions and second source and drain regions in the first and second semiconductor layers, respectively;

m) forming an interlayer insulating layer over said entire first surface of the insulating substrate;

n) etching the interlayer insulating layer to form first source and drain contact holes and second source and drain contact holes, the first source and drain contact holes exposing the first and second source and drain regions, the second source and drain contact holes exposing the second and second source and drain regions, respectively; and

o) forming source and drain electrodes, the source electrodes electrically connected to the first and second source regions through the first and second source contact holes, the drain electrodes electrically connected to the first and second drain regions through the first and second drain contact holes.

8. A thin film transistor manufactured by the method of claim 1.

9. A method of manufacturing a thin film transistor, comprising:

a) forming an amorphous silicon layer on an insulating substrate;

b) forming a first photoresist layer on the amorphous silicon layer while exposing edge portions of the amorphous silicon layer;

c) forming a metal layer over an entire first surface of the insulating substrate;

d) removing the first photoresist layer to expose a portion of the amorphous silicon layer under the first photoresist layer;

e) crystallizing the amorphous silicon layer to form a poly silicon layer metal induced lateral crystallization front;

f) a second photoresist layer having first and second photoresist patterns on the metal induced lateral crystallization front of the poly silicon layer to expose the metal induced lateral crystallization front, the first and second photoresist patterns spaced apart from each other;

g) etching the poly silicon layer using the first and second photoresist patterns as a mask to form first and second semiconductor layers and to remove the metal induced lateral crystallation front; and

h) removing the first and second photoresist patterns.

10. The method of claim 9, wherein the metal layer is made of Ni or Pd and has a thickness of 1 Å to 5000 Å.

11. The method of claim 9, further comprising, after the step (h), surface-treating the first and the second semiconductor layers.

12. The method of claim 11, wherein the surface treatment is performed using a dry-etching technique or an HF etching solution of 0.1 % to 20 %.

13. The method of claim 9, further comprising, after the step (h):

i) forming a gate insulating layer over said entire first surface of the insulating substrate;

j) forming a gate electrode on the gate insulating layer over the first and second semiconductor layers;

k) forming first source and drain regions and second source and drain regions in the first and second semiconductor layers, respectively;

l) forming an interlayer insulating layer over said entire first surface of the insulating substrate;

m) etching the interlayer insulating layer to form first source and drain contact holes and second source and drain contact holes, the first source and drain contact holes exposing the first and second source and drain regions, the second source and drain contact holes exposing the first and second source and drain regions, respectively; and

n) forming source and drain electrodes, the source electrodes electrically connected to the first and second source regions through the first and second source contact holes, the drain electrodes electrically connected to the first and second drain regions through the first and second drain contact holes.

14. A thin film transistor manufactured by the method of claim 11.

15. The method of claim 1, wherein in the step (g), a portion of the amorphous layer directly contacting the first metal layer is crystallized through a metal induced crystallization, and the remaining portion of the amorphous silicon layer is crystallized through a metal induced

lateral crystallization, so that a metal induced lateral crystallization front exists on a portion of the poly silicon layer between the first and second blocking patterns.

16. The method of claim 9, wherein in the step (e), a portion of the amorphous layer directly contacting the first metal layer is crystallized through a metal induced crystallization, and the remaining portion of the amorphous silicon layer is crystallized through a metal induced lateral crystallization, so that a metal induced lateral crystallization front exists on a metal induced lateral crystallization portion of the poly silicon layer crystallized by the metal induced lateral crystallization.

17. The method of claim 9, further comprising, after the step (g), removing the metal layer.